Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

What is claimed is:

1. (Currently Amended) An apparatus comprising:

a receiver to receive bytes of a data packet;

the receiver to transmit relevant bytes of the data packet and to identify irrelevant bytes of the data packet while receiving the bytes of the data packet, and wherein the receiver is operable to remove the identified irrelevant bytes of the data packet prior to transmitting the relevant bytes of the data packet; and

a data customer to receive only the relevant bytes of the data packet.

2. (Currently Amended) The apparatus of claim 1 ~~further comprising~~ wherein the receiver is operable to transmit the relevant bytes of the data packet prior to a receipt of an end of the data packet indication.

3. (Original) The apparatus of claim 1 wherein the irrelevant bytes are error correction code bytes.

4. (Currently Amended) The apparatus of claim 2 ~~further comprising~~ wherein the receiver is operable to identify the irrelevant bytes upon a receipt of an end of the data packet indication.

5. (Original) The apparatus of claim 1 wherein the irrelevant bytes are located at an end of the data packet.

6. (Original) The apparatus of claim 1 wherein the receiver comprises a circuit to identify the irrelevant bytes.

7. (Currently Amended) The apparatus of claim 1 wherein the receiver comprises ~~the~~ a circuit to delay transmitting of the bytes of the data packet by a predetermined number of bytes.

8. (Original) The apparatus of claim 7 wherein the predetermined number of bytes equals to a number of the irrelevant bytes.

9. (Original) A circuit comprising:

a plurality of storage elements to delay transmitting of bytes of a data packet by a predetermined number of bytes;

a first input signal to indicate presence of a valid byte of the data packet on an input data bus;

a second input signal to advance the byte through the plurality of storage elements; and

a third input signal to indicate an end of the data packet and to cancel advancement through the plurality of storage elements of bytes stored in the plurality of storage elements, the third input signal combined with the second input signal to indicate presence of an irrelevant byte on an output data bus.

10. (Original) The circuit of claim 9 further comprising:

a first output signal to indicate presence of a relevant byte of the data packet on the output data bus; and

a second output signal to indicate the end of the data packet.

11. (Currently Amended) The circuit of claim 10 wherein ~~a storage element~~ at least one of the plurality of storage elements is a flip flop.

12. (Currently Amended) The circuit of claim 10 wherein ~~a storage element~~ at least one of the plurality of storage elements is a latch.

13. (Original) The circuit of claim 10 wherein the predetermined number of bytes is a number of bytes representing an error correction code increased by one.

14. (Original) The circuit of claim 10 further comprising a plurality of multiplexers to control the plurality of storage elements.

15. (Original) The circuit of claim 10 wherein a total number of the plurality of the storage elements is equal to ((error correction code bytes +1) x a width of the input data bus) + ((error correction code bytes + 1) x 2).

16. (Original) The circuit of claim 14 wherein the second input signal and the third input signal control the first output signal by controlling output signals of the plurality of multiplexers.

17. (Original) The circuit of claim 10 wherein an asserted second input signal and an asserted third input signal de-assert the first output signal.

18. (Original) The circuit of claim 17 wherein the de-asserted first output signal indicates a presence of an irrelevant byte on the output data bus.

19. (Currently Amended) A method comprising:

receiving bytes of a data packet;

transmitting only relevant bytes of the data packet while receiving the bytes of the data packet; ~~and~~

identifying irrelevant bytes while receiving the bytes of the data packet; and

removing the identified irrelevant bytes of the data packet prior to transmitting the relevant bytes of the data packet.

20. (Original) The method of claim 19 wherein the receiving the bytes of the data packet is performed via an input bus.

21. (Original) The method of claim 19 wherein the transmitting the relevant bytes of the data packet comprises utilizing an output bus.

22. (Original) The method of claim 21 wherein the transmitting the relevant bytes of the data packet further comprises transmitting the relevant bytes to a data customer via an output bus.

23. (Original) The method of claim 22 wherein the transmitting the relevant bytes to the data customer comprises informing the data customer that the transmitted bytes are relevant.

24. (Original) The method of claim 23 wherein the informing the data customer is performed by asserting an output signal line.

25. (Original) The method of claim 19 wherein the transmitting the relevant bytes of the data packet is performed prior to receiving an end of the data packet indication.

26. (Original) The method of claim 19 wherein the irrelevant bytes are error correction code bytes.

27. (Original) The method of claim 19 wherein the identifying the irrelevant bytes is performed upon receiving an end of the data packet indication.

28. (Original) The method of claim 19 further comprises delaying the transmitting the relevant bytes by a predetermined number of bytes.

29. (Original) The method of claim 28 wherein the predetermined number of bytes equals to a one greater than a number of the irrelevant bytes.

30. (Original) The method of claim 29 wherein the delaying the transmitting the relevant bytes is performed by a circuit.

31. (Original) The method of claim 30 wherein the circuit comprises a plurality of storage elements.

32. (Original) The method of claim 31 wherein a total number of the plurality of the storage elements is equal to ((the number of irrelevant bytes +1) x a width of an input bus) + ((the number of the irrelevant bytes + 1) x 2)).

33. (Currently Amended) An apparatus comprising:

means for receiving bytes of a data packet;

means for transmitting relevant bytes of the data packet while receiving the bytes of the data packet; ~~and~~

means for identifying irrelevant bytes while receiving the bytes of the data packet; and

means for removing the identified irrelevant bytes of the data packet prior to transmitting the relevant bytes of the data packet.

34. (Original) The apparatus of claim 33 wherein the means for receiving the bytes of the data packet comprise means for receiving the bytes of the data packet via a bus.

35. (Original) The apparatus of claim 33 wherein the means for transmitting the relevant bytes of the data packet further comprise means for delaying the transmitting of the relevant bytes by a predetermined number of bytes.

36. (Original) The apparatus of claim 35 wherein the predetermined number of bytes equals to a one greater than a number of the irrelevant bytes.

37. (Original) The apparatus of claim 33 wherein the means for identifying the irrelevant bytes further comprise means for identifying the irrelevant bytes upon a receipt of an end of the data packet indication.

38. (Original) The apparatus of claim 37 wherein the means for transmitting the relevant bytes comprise means for informing a data customer that the transmitted bytes are relevant.

39. (Original) The apparatus of claim 38 wherein the means for informing the data customer comprise means for asserting an output signal line.